We Claim:

1. A method for writing to magnetoresistive memory cells of an MRAM memory, the magnetoresistive memory cells having a multilayer system containing layers stacked one above another, the layers including a soft-magnetic layer, a hard-magnetic layer and a tunnel oxide layer disposed between the soft-magnetic layer and the hard-magnetic layer, which comprises the steps of:

impressing write currents being in each case impressed on a respective word line and a respective bit line resulting in a superposition of magnetic fields generated by the write currents, and in each selected memory cell selected by the respective word line and the respective bit line, a magnetic field leads to a change of a magnetization direction of only the soft-magnetic layer, the write currents being impressed on the respective word line and the respective bit line in a manner temporally offset with respect to one another, resulting in the magnetization direction of the soft-magnetic layer in the selected memory cell being rotated in a plurality of successive steps in a direction desired for writing a logic "0" or "1".

2. The method according to claim 1, which further comprises

impressing the write currents for the selected memory cell in each case in approximately a same duration and in a manner temporally offset with respect to one another.

3. The method according to claim 1, which further comprises writing the logic "1" to the selected memory cell with a bit line write current of the respective bit line flowing in a same current flow direction as a word line write current of the respective word line and the bit line write current being impressed in a delayed manner relative to the word line write current of the respective word line.

4. An MRAM memory configuration, comprising:

an array containing magnetoresistive memory cells each having a multilayer system with layers stacked one above another, said layers including a soft-magnetic layer, a hard-magnetic layer, and a tunnel oxide layer disposed between said soft-magnetic layer and said hard-magnetic layer;

word lines;

bits lines crossing said word lines at each of said magnetoresistive memory cells; and

a writing control circuit for impressing write currents in each case onto a respective word line and a respective bit line of a respective memory cell selected for writing, said writing control circuit having a write circuit for impressing the write currents in each case on said respective word line and said respective bit line in a manner temporally offset with respect to one another, resulting in a magnetization direction of only said soft-magnetic layer of said respective memory cell being rotated in a plurality of successive steps in a direction desired for writing a logic "0" or "1".